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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/072,415	02/05/2002	Ji Ung Lee	MI30-068	5182

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EXAMINER	
FULK, STEVEN J	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 02/01/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H'A

Office Action Summary	Application No.	Applicant(s)	
	10/072,415	LEE ET AL.	
	Examiner	Art Unit	
	Steven J. Fulk	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *74-86,88-96,102-111,113,114 and 116-119* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *74-86,88-96,102-111,113,114 and 116-119* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 February 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2-5-02
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

2. Applicant's amendment, filed September 15, 2005, which cancels claims 1-73, 87, 97-101, 112, and 115 and adds claims 116-119 has been entered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 74, 77-78, 83, 85, 88-90, 92, 113-114, 116-117 and 119 are rejected under 35 U.S.C. 102(e) as being anticipated by Hirano et al. '318.

Hirano et al. discloses a field emission transistor device fabrication method comprising providing semiconductive material (fig. 5, 18) including a channel region (between 14b and 17); providing a source semiconductive region (17) and a drain semiconductive region (14b) adjacent to the channel region of the semiconductive

material, and wherein the providing the drain semiconductive region comprise providing a plurality of emitters (14; col. 5, lines 64-67).

The reference further discloses providing gate dielectric material over the channel region (fig. 5, 12a); providing a gate over the gate dielectric material and the channel region (13a), the gate being intermediate the source and drain semiconductive regions to form a field effect transistor and the gate formed about the emitters; and forming the drain semiconductive region and the emitters by etching to comprise a monolithic semiconductive material (col. 5, lines 24-28, 44-48).

Hirano et al. further discloses a field emission operational method comprising controlling the current flow intermediate the source and drain regions within the channel region and controlling emission of electrons from the field emitter using the gate intermediate the source and drain regions (col. 6, lines 7-21).

5. Claims 79-82, 93-96, 102-106, 108, 109 and 111 are rejected under 35 U.S.C. 102(e) as being anticipated by Gardner et al. '894.

Gardner et al. discloses a field effect transistor fabrication method comprising providing a thin film semiconductive layer (fig. 1A, 102; epi layer, col. 5, lines 20-26) including a channel region (fig. 1F, 118); providing a plurality of spaced semiconductive regions adjacent to the channel region of the semiconductive layer (fig. 1F, 110A & 110B); and self-aligning a gate intermediate of the semiconductive regions without the use of a mask by providing a gate dielectric material over the channel region (fig. 1H, 130), providing a gate material over the gate dielectric (fig. 1I, 136), and chemical-mechanical polishing the gate dielectric and gate material to

result in upper surfaces of the gate dielectric material and semiconductive regions to be substantially elevationally coincident with an upper surface of the gate (fig. 1J).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 75-76, 84, 86, 91, 107, 110 and 118 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hirano et al. '318 in view of Gardner et al. '894.

a. Regarding claims 75, 84, and 91, Hirano et al. teaches all of the elements of the claims as discussed above including forming a field effect device with a semiconductive material, but the reference does not explicitly teach the semiconductive material to be a thin film semiconductive layer.

Gardner et al. teaches a method of forming a field effect device wherein the semiconductive material is a thin film semiconductive layer (fig. 1A, 102; epi layer, col. 5, lines 20-26).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Hirano et al. using the thin film semiconductive material of Gardner et al. One would have been motivated to do this because thin film epitaxial layers were conventionally used in field effect devices due to the ability to precisely control the crystal

orientation, doping and resistivity of the epitaxial layer to improve the performance of the device (Gardner et al., col. 5, lines 20-26).

b. Regarding claims 76, 107, and 110, Hirano et al. teaches all of the elements of the claims as discussed above including forming a field effect transistor with a gate intermediate of a source region and a drain/field emitter region, but the reference does not explicitly teach forming the gate without the use of a mask by polishing the gate dielectric and gate material.

Gardner et al. teaches a method of forming a field effect device wherein the gate is formed without the use of a mask by polishing the gate dielectric (fig. 1I, 130) and gate material (fig. 1I, 136; fig. 1J).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the device of Hirano et al. using the gate polishing method of Gardner et al. One would have been motivated to do this because polishing the gate would have resulted in a planarized transistor surface, thus reducing the surface non-uniformities that interfere with subsequent lithography steps and improving the process yield of the devices (Gardner et al., col. 2, lines 34-45).

c. Regarding claims 86 and 118, Hirano et al. teaches all of the elements of the claims as discussed above including forming a field effect transistor with a gate intermediate of a source region and a drain/field emitter region and forming the tip of the emitter elevationally below the upper surface of the gate (fig. 5, emitter tip 14 and gate 13a), but the reference does not

explicitly teach forming an elevated source region such that the tip of the emitter is elevationally below an upper surface of source.

Gardner et al. teaches forming an elevated source region of a field effect transistor in order to form a planarized transistor surface (fig. 1J, 110A).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the field effect transistor device of Hirano et al. using the raised source of Gardner et al. One would have been motivated to do this because using a source that extends to the surface of the gate and above the tip of the emitter/drain region, as opposed to a flat source region below the gate surface, would have resulted in a more planarized transistor surface, thus reducing the surface non-uniformities that interfere with subsequent lithography steps and improving the process yield of the devices (Gardner et al., col. 2, lines 34-45).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Kane '426, Kanemaru et al. '478, and Itoh et al. '595 disclose methods of forming field emission transistor devices.

Smith et al. '887, Komatsu '682, Lee et al. '707, Takada et al. '972, and Moradi et al. '229 disclose methods of forming field emitter devices by etching.

Inaba '258, Gardner et al. '025, and Gardner et al. '167 disclose methods of forming field effect transistors with self-aligned gates by polishing the gate dielectric and gate material.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven J. Fulk whose telephone number is (571) 272-8323. The examiner can normally be reached on Monday through Friday, 9:00am to 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bill Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
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Art Unit 2891

January 26, 2006